REMARKS

In the Office Action of November 16, 2004, claims 1-26 were rejected under 35 U.S.C. 102(b) as being anticipated by Sherman et al. (U.S. Patent No. 5,175,830), hereinafter Sherman. Claim 1 is directed to

> An apparatus for reducing the memory footprint of a first processor device, the apparatus comprising:
> a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece;
> a storage area for storing certain pieces of the program code;
> a first memory area associated with the first processor device for receiving certain portions of the program code; and
> a hardware transfer mechanism for efficiently linking the storage area with the first memory area,
> wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area.

The Examiner asserted that claim1 is disclosed in Sherman, column 1, lines 65-67; column 2, lines 6-27; and column 3, lines 38-60. Applicant respectfully submits that Sherman involves "differentiating the overlays into a *code portion* and into a *data portion*" (column 1, lines 65-66, emphasis added). Claim 1, in contrast, refers to "a segment of program code which is split into at least one *controlling piece* and at least one separate *working piece*" (emphasis added). Differentiating an *overlay* into a *code portion* and a *data portion* is not the same as splitting a segment of *code* into a *controlling piece of code* and a *working piece of code*. Therefore, Applicant respectfully submits that claim 1, and claims 2-12 depending therefrom, are not anticipated by Sherman.

Additionally, Applicant submits that Sherman does not disclose "a hardware transfer mechanism for efficiently linking the storage area with the first memory area," as called for in claim 1. The Examiner did not specify which portion of Sherman is deemed to anticipate this element of claim 1, but Applicant will assume that the excerpt at column 3, lines 38-60, is the portion that Examiner deems to anticipate this element. Column 3, lines 38-60 refer to a Load

and Control System 10 that "determines which program modules, or Overlays, typically stored on a mass store 9 such as a disk, are to be loaded in support of a particular application program being run." Applicant submits that said Load and Control System 10 resides in a region 6 of the physical memory space 1 (see col. 3, lines 41-43), and is therefore software, not hardware, as called for in the instant element of claim 1. Therefore, Applicant submits that claim 1, and claims 2-12 depending therefrom, further distinguish over Sherman.

The Examiner also rejected claims 13-26 as anticipated by Sherman for the same reasons used to reject claims 1-12. Therefore, Applicant submits that claims 13-26 are not anticipated by Sherman for the same reasons set out above with respect to claims 1-12.

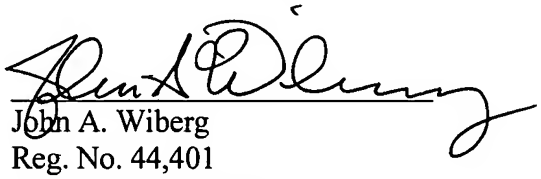
Claim 26 was also rejected under 35 U.S.C. 102(e) as being anticipated by Chin et al. (U.S. Patent No. 6,608,625) or Jacobs et al. (U.S. Patent No. 6,385,678). Claim 26 is amended herewith to indicate that the digital signal processor is associated with the network telephone device. Applicant submits that claim 26 as amended is not anticipated by Chin or Jacobs.

In view of the foregoing, Applicant requests allowance of claims 1-26.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: February 16, 2005

Respectfully submitted,



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